REMARKS

Information Disclosure Statements

Applicant has received an initialed copy of the Form PTO/SB/08A submitted with the IDS dated April 5, 2005. However, Applicant did not receive an initialed copy of the same form submitted with the IDS dated September 19, 2003. A copy of the un-initialed form is attached to this Amendment, and an initialed copy is requested.

Claim Rejections Under 35 USC §102 And 35 USC §103

Claims 1-9, 11, 12, 14-16, 75, 81, 84, 86 and 87 have been rejected under 35 USC §102(b) as being anticipated by Alcoe et al. (US Patent No. 5,760,465).

Claims 10, 13, 17, 18, 19, 76, and 83-85 have been rejected under 35 USC 103(a) as being unpatentable over Alcoe as applied to claims 1-9, 11, 12, 14-16, 75, 81, 83, 84, 86 and 87 above, and further in view of Siu (US Patent No. 6,664,617 B2).

Claims 77-80 and 82 have been rejected under 35 USC 103(a) as being unpatentable over Alcoe as applied to claims 1-9, 11, 12, 14-16, 75, 81, 83, 84, 86, and 87 above and further in view of Muthukumaraswamy et al. (US Patent No. 6,229,227 B1).

The rejections under 35 USC §102, and 35 USC §103 are traversed for the reasons to follow.

Summary of the Invention

Claims 1-19 are directed to a semiconductor component 10 (Figure 1C). As shown in Figure 1C, the component 10 includes a stiffener 12 and a circuit decal 16 attached to the stiffener 12. The component 10 also includes a

semiconductor die 14 attached to the stiffener 12 in a board on chip configuration (BOC), and wire interconnects 18 in electrical communication with the die 14 and the circuit decal 16.

The circuit decal 16 does not include a polymer substrate as with a conventional flexible circuit for a semiconductor component. Rather, the circuit decal 16 includes a pattern of metal conductors 40 having contacts 44 in an area array, and a polymer mask layer 34 on the conductors 40. In addition, an adhesive layer 32 attaches the circuit decal 16 to the stiffener 12, and electrically insulates the conductors 40 from the stiffener 12. The component 10 also includes terminal contacts 20 on the contacts 44 electrically isolated by the mask layer 34, a die encapsulant 38 encapsulating the die 14, and an interconnect encapsulant 22 encapsulating the wire interconnects 18. The polymer mask layer 34 thus serves the functions of a solder mask for the terminal contacts 20, a support layer for the conductors 40, and a protective outer layer for the component 10.

Claims 75-87 are directed to systems 60 (Figure 7B), or 70 (Figure 8), or 72 (Figure 9), or 74 (Figure 10), or 76 (Figure 11), which include the component 10 (Figure 1C).

Argument

The rejections under 35 USC §102 are traversed as Alcoe et al. does not disclose or enable all of the features of the claimed component and system. In this regard, a proper 35 USC §102 rejection requires that each and every limitation of the claimed invention be disclosed in a single prior art reference. In addition, the reference must be enabling and describe the applicant's

claimed invention sufficiently to have placed it in possession of a person of ordinary skill in the field of the invention. In re David C. Paulsen, 30 F.3d 1475, 31 USPQ 2d (BNA) 1671, (U.S. App 1994).

The rejections under 35 USC §103 are traversed because the combinations of Alcoe et al. and Siu, and Alcoe, Siu and Muthukumaraswamy et al. do not disclose or all of the features of the claimed component and system as required by MPEP 2142, 2143. However, the claims have been amended to further emphasize the features which make the component and the system novel and unobvious over the art.

The claimed component 10 (Figure 1C) includes the circuit decal 16 (Figure 1C) which comprises only two layers, a metallization layer 36 (Figure 1C) with the conductors 40 (Figure 1C), and the polymer mask layer 34 (Figure 1C). In support of the rejections under 35 USC §102 and 35 USC §103, the dielectric layer 29 in Figure 1 of Alcoe et al. was deemed to be equivalent to the polymer mask layer 34 of the present component 10. However, the dielectric layer 29 in Alcoe et al. has a different structure, and a different function, than the polymer mask layer 34 of the present component 10. Specifically, in Alcoe et al. the dielectric layer 29 comprises polyimide (column 6, lines 3), and forms the substrate for the flexible circuitized substrate 15.

In the art of semiconductor packaging, substrates and masks are different elements of a component, which perform different functions. In this regard, the main purpose of a polymer substrate is to provide flexible support for conductors, whereas the main purpose of a polymer mask for terminal contacts is to provide electrical isolation and a solder barrier between the terminal contacts. The present

component 10 includes a circuit decal 16 (Figure 1C) which does not have a flexible substrate, but rather conductors 40 (Figure 1C) which attach directly to the stiffener 12. This provides an improved and simplified component 10, which can be made thinner because it does not include a separate polymer substrate.

In contrast, the package 11 (Figure 1) in Alcoe et al. includes the dielectric layer 29 which functions as a polymer substrate, and a second dielectric layer 41 which functions as a mask material (column 7, lines 29-37). The dielectric layer 29 in the Alcoe et al. package 11 is conventional in the art. The present component eliminates the dielectric layer 29, which makes the component thinner and simpler. This claimed construction exhibits an insight running contrary to the teachings of the prior art.

Each of the independent claims (claims 1, 7, 11, 75 and 81) has been amended to include additional limitations intended to distinguish the claimed component having conductors on a polymer mask layer, from a conventional component having conductors on a polymer substrate with an additional polymer mask layer.

Claim 1 has been amended to recite "a circuit decal having only two layers including a plurality of conductors in physical contact with the adhesive layer having a plurality of contacts in an area array, and a polymer mask on the conductors having a plurality of openings aligned with the contacts". Claim 1 also recites "the polymer mask configured as a solder mask for the terminal contacts and a support structure for the conductors." Antecedent basis for the additional recitations is contained on page 3, lines 15-18, on page 10, lines 9-13, and on page 19, lines 1-12 of the specification. Claim 1 thus defines a

component having conductors with a polymer mask, but without a separate polymer substrate for supporting the conductors.

Claim 7 has been amended to recite "the polymer mask configured as a solder mask for the terminal contacts, an outer electrically insulating layer for the conductors and the component, and a support structure for the circuit decal in place of a separate polymer substrate." Antecedent basis for this recitation is contained on page 10, lines 9-13 of the specification. In Alcoe et al., neither the dielectric layer 29, nor the second dielectric layer 41, have the recited configuration. Rather, both the dielectric layer 29 and the second dielectric layer 41 are required.

Claim 11 has been amended to recite the polymer layer comprises "only two layers", including "an imageable resist configured as a solder mask and a support structure for the conductors in place of a separate polymer substrate". Antecedent basis for the term "solder mask" is contained on page 10, line 10 of the specification. Antecedent basis for the term "imageable resist" is contained on page 19, lines 23-25 of the specification. In Alcoe et al., the dielectric layer 29 provides support for the conductors 23, but does not function as a solder mask, and does not comprise an imageable resist. Although the second dielectric layer 41 functions as a solder mask, it does not provide support for the conductors 23 in place of a separate polymer substrate.

Claim 75 recites that the polymer mask comprises an "imageable resist". Antecedent basis for the term "imageable resist" is contained on page 19, lines 23-25 of the specification. In addition, claim 75 recites "the polymer mask configured as a solder mask for the terminal

contacts, an outer electrically insulating layer for the conductors and the component, and a support structure for the circuit decal in place of a separate polymer substrate." Antecedent basis for these recitations is contained on page 10, lines 9-13 of the specification.

Claim 81 recites the polymer layer comprises "an imageable resist configured to provide a solder mask and to support the conductors in place of a separate polymer substrate". Claim 81 also recites "the stiffener and the component have a footprint of less than 1.25X an outline of the die". In addition, similar "chip scale" size recitations are contained in dependent claims 2, 3 and 12. Antecedent basis for these recitations is contained on page 23, lines 12-19 of the specification. These size recitations further distinguish the claimed component and system from the package 11 (Figure 1) in Alcoe et al. Specifically, the Alcoe et al. package 11 (Figure 1) does not have a chip scale outline, and the stiffener 13 (Figure 1) is much larger than the die 19 (See Figure 2(B) of Alcoe et al.).

With respect to the 35 USC §103 rejections, the combination of Alcoe et al. and Siu does not disclose the above noted limitations of the amended claims. Similarly, the combination of Alcoe et al., Siu and Muthukumaraswamy et al. does not disclose the above noted limitations of the amended claims. Each of the rejected dependent claims is thus submitted to be novel over Alcoe et al., and unobvious over Alcoe et al. in combination with the prior art.

CONCLUSION

In view of the amendments and arguments, favorable consideration and allowance of claims 1-19 and 75-87 is requested. Should any issues remain, the Examiner is requested to contact the undersigned by telephone.

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AUGUST 2, 2005
Date of Signature

Stephen A. Gratton, Attorney for Applicant